WHAT IS CLAIMED IS:

1. A processor chip, comprising:

a processing core; and

at least one bank of DRAM memory, including a mode control input for controlling the mode of said at least one bank of DRAM memory between a first mode and a second mode, wherein when said at least one bank of DRAM memory is in said first mode, said at least one bank of DRAM memory acts as physical memory, and when said at least one bank of DRAM memory is in said second mode, said at least one bank of DRAM memory acts as cache memory.

2. The processor chip as recited in claim 1, wherein said processor chip is a first processor chip which further comprises:

an I/O link configured to communicate with other processor chips; and

a communication and memory controller in electrical communication with said processing core, said at least one bank of memory, and said I/O link;

said communication and memory controller for controlling the exchange of data between said first processor chip and said other processor chips, and for receiving memory requests from said processing core on said first processor chip and from other processing cores on said other processor chips via said I/O link, and processing said memory requests with said at least one bank of memory.

3. The processor chip as recited in claim 2, wherein said communication and memory controller comprises:

a first memory controller in electrical communication with said processing core and said at least one bank of memory; and

a second memory controller in electrical communication with said first memory controller and said I/O link;

said second memory controller for controlling the exchange of data between said first processor chip and said other processor chips;

said first memory controller for receiving memory requests from said processing core on said first processor chip and said second memory controller, and process said memory requests with said at least one bank of memory.

4. The processor chip as recited in claim 2, wherein when said at least one bank of memory on said first processor chip and said at least one bank of memory on said

other processor chips comprise physical memory, the data stored on said at least one bank of memory on said first processor chip is different from the data stored on said at least one bank of memory on said other processor chips.

5. The processor chip as recited in claim 2, further comprising an external memory interface in electrical communication with said communication and memory controller;

said external memory interface for connecting said first processor chip in electrical communication with external memory; and

said communication and memory controller for receiving memory requests from said processing core on said first processor chip and from processing cores on said other processor chips, determining whether said memory requests are directed to said at least on bank of memory on said first processor chip, to said at least one bank or memory on said other processor chips, or to said external memory, and processing said memory requests with said at least one bank of memory on said first processor chip, with said at least one bank of memory on said other processor chips through said I/O link, or with said external memory through said external memory interface.

6. The processor chip as recited in claim 5, wherein said external memory is DRAM.

7. The processor chip as recited in claim 5, wherein when said at least one bank of memory on said first processor chip and said at least one bank of memory on said other processor chips comprise physical memory, the data stored on said at least one bank of memory on said first processor chip is different from the data stored on said at least one bank of memory on said other processor chips and said external memory.

8. In a computer system, a scalable computer processing architecture, comprising:

one or more processor chips, each comprising:

a processing core;

at least one bank of DRAM memory including a mode control input for controlling the mode of said at least one bank of DRAM memory between a first mode and a second mode, wherein when said at least one bank of DRAM memory is in said first mode, said at least one bank of memory acts as physical memory, and when said at least one bank of

DRAM memory is in said second mode, said at least one bank of DRAM memory acts as cache memory;

an I/O link configured to communicate with other of said one or more processor chips or with I/O devices;

a communication and memory controller in electrical communication with said processing core, said at least one bank of memory, and said I/O link;

said communication and memory controller for controlling the exchange of data between said one or more processor chips and I/O devices, and for receiving memory requests from said processing cores on said one or more processor chips and from said I/O devices, and processing said memory requests with said at least one bank of memory.

wherein said computer processing architecture can be scaled larger by connecting together two or more of said processor chips in parallel via said I/O links of said processor chips, so as to create multiple processing core pipelines which share data therebetween.

9. The processor chip as recited in claim 8, wherein said communication and memory controller on said one or more processor chips comprises:

a first memory controller in electrical communication with said processing core and said at least one bank of memory; and

a second memory controller in electrical communication with said first memory controller and said I/O link;

said second memory controller for controlling the exchange of data between said processor chip and said other processor chips;

said first memory controller for receiving memory requests from said processing core and said second memory controller, and process said memory requests with said at least one bank of memory.

10. The processor chip as recited in claim 8, wherein when said at least one bank of memory on said one or more processor chips comprise physical memory, the data stored on said at least one bank of memory on each of said one or more processor chips is different from the data stored on said at least one bank of memory on each of the other of said one or more processor chips.

11. The computer processing architecture as recited in claim 8, wherein at least one of said one or more processor chips further comprises an external memory interface in electrical communication with said communication and memory controller;

said external memory interface for connecting said at least one of said one or more processor chips in electrical communication with external memory; and

said communication and memory controller of said at least one of said one or more processor chips for receiving memory requests from said processing cores of said one or more processor chips and said I/O devices, determining whether said memory requests are directed to said at least one bank of memory on said at least one of said one or more processor chips, to other of said one or more processor chips, or to said external memory, and processing said memory requests with said at least one bank of memory on said at least one of said one or more processor chips, with said other of said one or more processor chips, or with said external memory through said external memory interface.

12. The computer processing architecture as recited in claim 11, wherein said external memory comprises DRAM.

13. The processor chip as recited in claim 11, wherein when said at least one bank of memory on said one or more processor chips comprise physical memory, the data stored on said at least one bank of memory on each of said one or more processor chips is different from the data stored on said at least one bank of memory on each of the other of said one or more processor chips and said external memory.

14. The computer processing architecture as recited in claim 8, comprising a first and a second processor chip, wherein said processing core on said first processor chip is configured to access said at least one bank of memory on said second processor chip through the I/O links of said first and said second processor chips.

15. The computer processing architecture as recited in claim 14, wherein a memory request directed from said processing core on said first processor chip to said at least one bank of memory on said second processor chip is processed by:

said processing core on said first processor chip sending a memory request to said communication and memory controller on said first processor chip;

said communication and memory controller on said first processor chip determining that said memory request is not accessing said at least one bank of memory on

said first processor chip, and passing said memory request to said communication and memory controller on said second processor chip via said I/O links on said first and said second processor chips;

said communication and memory controller on said second processor chip processing said memory request with said at least one bank of memory on said second processor chip by performing a memory access function with said at least one bank of memory on said second processor chip;

said communication and memory controller on said second processor chip passing a result of said memory access function back to said communication and memory controller on said first processor chip via said I/O links on said first and said second processor chips; and

said communication and memory controller on said first processor chip communicating said result of said memory access function to said processing core on said first processor chip.

16. In a computer architecture having a plurality of processor chips, each comprising a processing core and at least one bank of memory, a method for a first processing core on a first processor chip of accessing said at least one bank of memory on a second processor chip, comprising the steps of:

said first processing core on said first processor chip issuing a memory request;

determining whether said memory request is accessing data in said at least one bank of memory on said first processor chip or data in said at least one bank of memory on said second processor chip;

if said memory request is accessing data in said at least one bank of memory on said second processor chip, communicating said memory request to said second processor chip;

performing a memory access function to said at least one bank of memory on said second processor chip; and

communicating a result of said memory access function back to said first processing chip.

17. The method as recited in claim 16, wherein said at least one bank or memory on each of said plurality of processing chips comprises physical memory.

18. The method as recited in claim 16, wherein said at least one bank of memory on each of said plurality of processing chips comprises cache memory.

19. The method as recited in claim 16, wherein said at least one bank of memory on each of said plurality of processing chips further comprises a mode control input, and wherein said at least one bank of memory on each of said plurality of processing chips can switch between physical memory and cache memory by enabling or disabling said mode control input.